Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.160”**

**.128”**

**SOURCE**

**GATE**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size:**

**Backside Potential: DRAIN**

**Mask Ref: HEX-3 100V N-Channel**

**APPROVED BY: DK DIE SIZE .128” X .160” DATE: 11/9/21**

**MFG: INT’L RECTIFIER THICKNESS .014” P/N: IRFC540**

**DG 10.1.2**

#### Rev B, 7/19/02